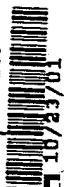


10/015169



PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10015169	FILING DATE 10/23/2001	CLASS 387	SUBCLASS 64	GAU 2816	EXAMINER SARAS Anyaso
**APPLICANTS: Kawahata Ken; Yamada Yukimitsu; <div style="text-align: center; font-size: 1.2em;">345 98 2675</div>					
**CONTINUING DATA VERIFIED:					
** FOREIGN APPLICATIONS VERIFIED: JAPAN 2000-324496 10/24/2000 JAPAN 2001-208160 07/09/2001					
PG-PUB <input type="checkbox"/> DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no		35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO	
Verified and Acknowledged Examiners's initials				9281-4195	
TITLE : Shift register circuit including first shift register having plurality of stages connected in cascade and second shift register having more stages					
U.S. DEPT. OF COMM./PAT. & TM-PTO-436L (Rev. 12-94)					

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G.
ISSUE FEE		Primary Examiner	DRAWING	
Amount Due	Date Paid		Sheets Drwg.	Figs. Drwg.
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner	
		WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.		

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